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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/072,169	02/07/2002	Gregory M. Wright	16159.072001	1320

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EXAMINER	
MCLEAN MAYO, KIMBERLY N	
ART UNIT	**PAPER NUMBER**
2187	13

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/072,169	Applicant(s) WRIGHT ET AL.	
	Examiner Kimberly N. McLean-Mayo	Art Unit 2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The enclosed detailed action is in response to the Information Disclosure Statement submitted on January 29, 2004 and the Amendment submitted on February 19, 2004.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-9 and 19-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Henderson et al. (USPN: 6,446,188) in view of Witt (USPN: 6,240,484).

Regarding claims 1, 3-4, 7 and 9, Henderson discloses a computer system comprising a processor (Figure 2A); a processor (Figure 2A, Reference 204); an object cache operatively connected to the processor (Figure 2A, Reference 210); a memory (Figure 2A, memory coupled to Reference 206; C 4, L 66); a translator to map an object address, (which is generated by the processor using the addressing format of the system [extended address encoding], which embeds [maps] the address into an unused part of a physical address range), to a physical address within the memory, thereby converting operations using the object address into operations using the physical address (Figure 3A, Reference 310; C 3, L 15-20; C 5, L 28-30). Henderson does not explicitly disclose the translator interposed between the object cache and the memory. However, Witt teaches the concept of a translator located between a cache and memory. This feature taught by Witt provides efficiency by performing translations only upon the occurrence of a

cache miss in oppose to performing translations for every memory access. Hence, it would have been obvious to one of ordinary skill in the art to use the teachings of Witt with the system taught by Henderson for the desirable purpose of efficiency.

Regarding claim 2, Henderson discloses the object address comprising an object identification number and an offset (refer to Figure 3A, References 308a – 308c).

Regarding claim 5, Henderson discloses the translator mapping the object address to the physical address using a table (Figure 3A, Reference 316).

Regarding claim 6, Henderson discloses using an extended instruction set (the instruction set of the processor is interpreted as the extended instruction set).

Regarding claim 8, Henderson discloses loading a plurality of cache lines from the memory (when plural cache misses occur, plural cache lines are retrieved from main memory and loaded into the cache memory).

Regarding claims 19-20, 25, 28-29 and 34, Henderson discloses a method for retrieving an object comprising obtaining an object address corresponding to the object (object address is obtained from the virtual address output from a processor); determining if the object address corresponds to a tag in a tag array of a cache and retrieving the object address if the tag corresponding to the object address is in the tag array (C 7, L 10-20); and retrieving a cache line [from main memory]

using the physical address if the object address is not in the tag array and entering the cache line into the cache (when a cache miss occurs a cache line is retrieved from main memory). Henderson does not explicitly teach translating the object address into a physical address if the object address is not in the tag array using a translator. However, Witt teaches translating an address into a physical address if the address is not in the tag array using a translator (C 10, L 32-58). This feature taught by Witt provides efficiency by performing translations only upon the occurrence of a cache miss in oppose to performing translations for every memory access. Hence, it would have been obvious to one of ordinary skill in the art to use the teachings of Witt with the system taught by Henderson for the desirable purpose of efficiency. Additionally, regarding claim 28, Henderson and Witt do not teach the above features in a multiprocessor environment. However, it is well known in the art to use multiple processors in a system for the desirable purpose of increased performance and hence, for this reason, it would be obvious to one of ordinary skill in the art to implement the above features in a multiprocessor environment.

Regarding claims 21-22 and 30-31, Henderson discloses the object address comprising an object identification number and an offset (refer to Figure 3A, References 308a – 308c).

Regarding claims 23-24, 26, 32-33 and 35, Henderson discloses an object address, (which is generated by the processor using the addressing format of the system [extended address encoding], which embeds [maps] the address into an unused part of a physical address range), to a physical address within the memory, thereby converting operations using the object address

into operations using the physical address (Figure 3A, Reference 310; C 3, L 15-20; C 5, L 28-30).

Regarding claims 27 and 36, Henderson discloses loading a plurality of cache lines from the memory (when plural cache misses occur, plural cache lines are retrieved from main memory and loaded into the cache memory).

4. Claims 10-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over in view of Henderson et al. (USPN: 6,446,188) in view of Witt (USPN: 6,240,484) and Frank (PGPUB: US 2002/0178341)

Regarding claims 10, 12-13, 16 and 18, Henderson discloses a computer system comprising a processor (Figure 2A, Reference 204); an object cache connected operatively to the processor (Figure 2A, Reference 210); a memory (Figure 2A, memory coupled to Reference 206; C 4, L 66); a translator to maps an object address, (which is generated by the processor using the addressing format of the system [extended address encoding], which embeds [maps] the address into an unused part of a physical address range), to a physical address within the memory, thereby converting operations using the object address into operations using the physical address (Figure 3A, Reference 310; C 3, L 15-20; C 5, L 28-30). Henderson does not disclose the translator interposed between the cache and the memory nor does Henderson disclose the computer system comprising a plurality of processors operatively connected to the cache. However, Witt teaches the concept of a translator located between a cache and memory. This feature taught by Witt provides efficiency by performing translations only upon the occurrence

of a cache miss in oppose to performing translations for every memory access. Additionally, Frank discloses a computer system (Figure 3) comprising a plurality of processors (Figure 3, References labeled Computer, such as References 108 and 120); an object cache operatively connected to the plurality of processors (Figure 3, Reference 112). Multiple processors in a system increase the performance of the system by providing multiple processing elements to process data. Hence, it would have been obvious to one of ordinary skill in the art to use the teachings of Witt and Frank with the system taught by Henderson for the desirable purpose of efficiency and improved performance.

Regarding claim 11, the system taught by Henderson, Witt and Frank discloses the object address comprising an object identification number and an offset (Henderson - refer to Figure 3A, References 308a – 308c).

Regarding claim 14, the system taught by Henderson, Witt and Frank discloses the translator mapping the object address to the physical address using a table (Figure 3A, Reference 316).

Regarding claim 15, the system taught by Henderson, Witt and Frank discloses using an extended instruction set (the instruction set of the processors is interpreted as the extended instruction set).

Regarding claim 17, the system taught by Henderson, Witt and Frank discloses loading a plurality of cache lines from the memory (when plural cache misses occur, plural cache lines are retrieved from main memory and loaded into the cache memory).

Response to Arguments

5. Applicant's arguments filed have been fully considered but they are not persuasive. Regarding Applicant's argument with respect to Witt, Witt is not relied upon for translating between object addresses and physical addresses. Witt is relied upon for teaching interposing a translator (Reference 420 in Figure 9 within Reference 164 in Figure 1) between a cache (Figure 1, Reference 104, 150) and memory (Figure 1, Reference 101).

Regarding Applicant's argument with respect to claims 19 and 28, the claim language does not state translating the object address to a physical address only if the object address is not in the tag array. The Examiner disagrees with the contention that Henderson teaches away from doing so. This inference is not just simply because the inventor implements something different; the inventor in this case merely does not teach the claimed limitation. Hence, this is why the claim was rejected under 35 U.S.C 103.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimberly N. McLean-Mayo whose telephone number is 703-308-9592. The examiner can normally be reached on M-F (9:00 - 6:30) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 703-308-1756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kimberly N. McLean-Mayo

Examiner
Art Unit 2187

KIMBERLY MCLEAN-MAYO
PRIMARY EXAMINER

KNM

April 24, 2004